

FIG.1

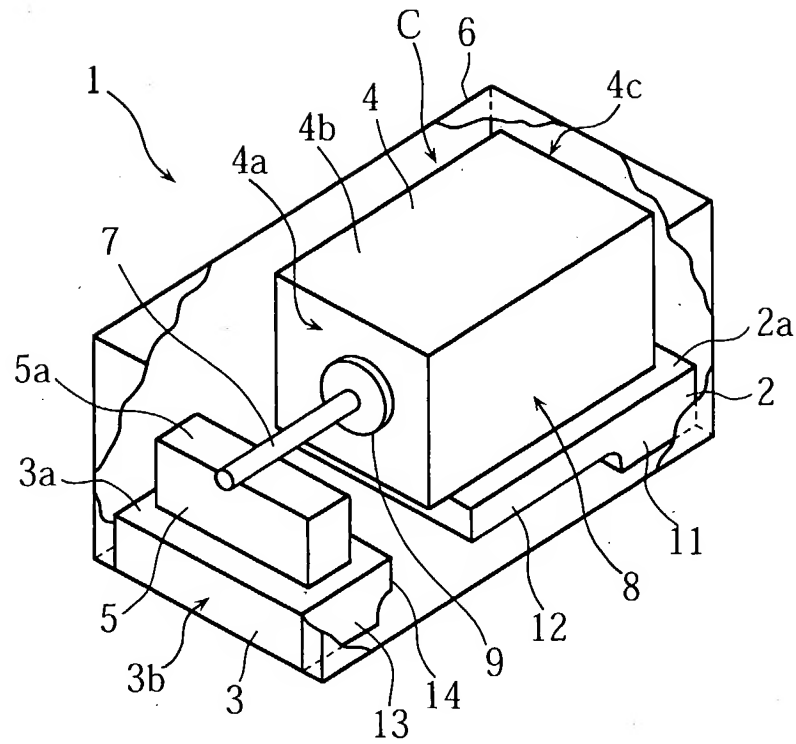


FIG.2

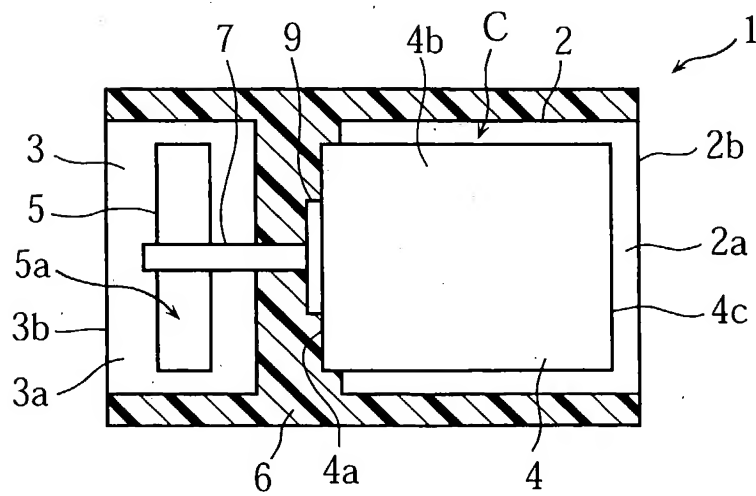


Figure 1 is a plan view of the first embodiment of the semiconductor device. It shows a rectangular substrate 1 with a central rectangular region 6. On the left side of region 6, there is a rectangular region 3, and on the right side, there is a rectangular region 2. The bottom edge of region 3 is labeled 3c, and the bottom edge of region 2 is labeled 2c.

FIG.5

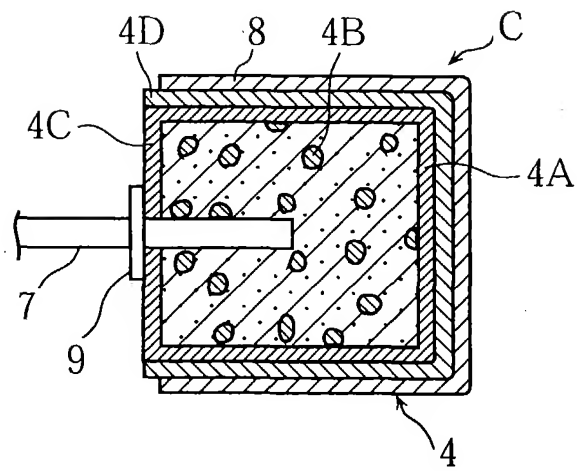


FIG.6

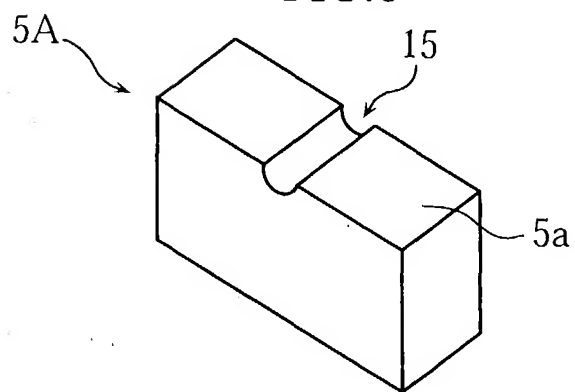


FIG.7

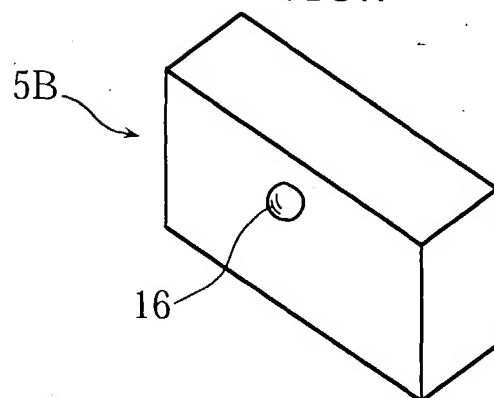


FIG.8

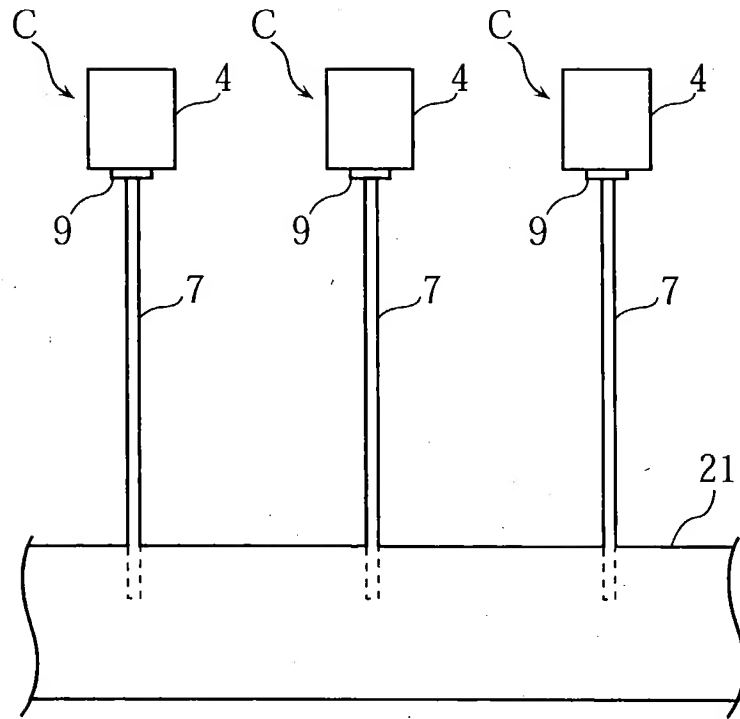


FIG.9

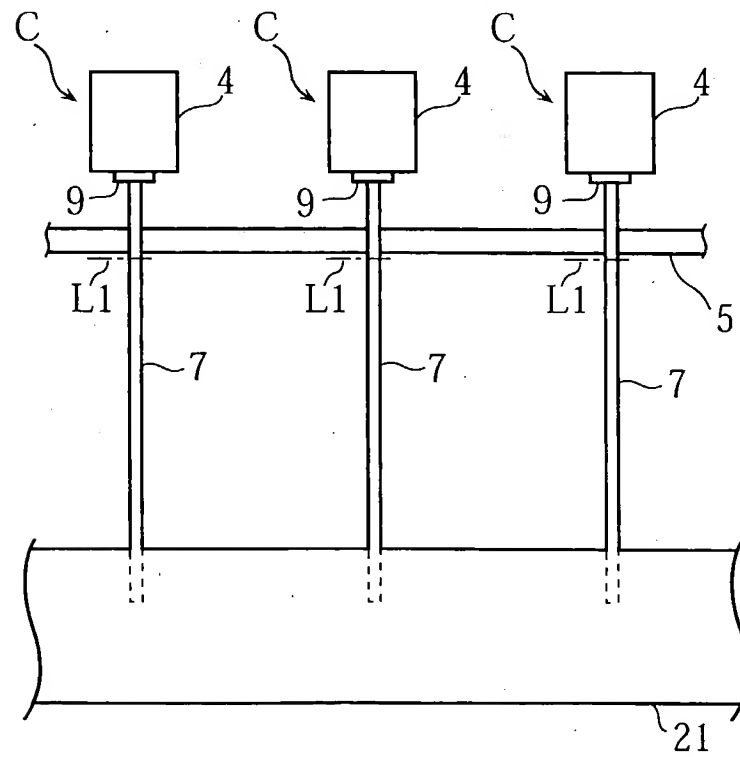


FIG.10

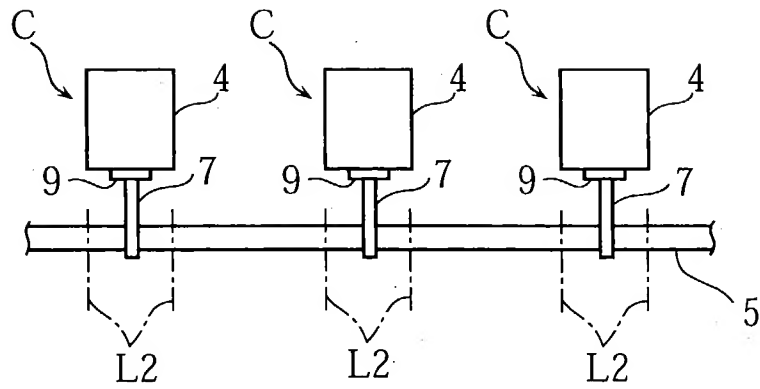


FIG.11

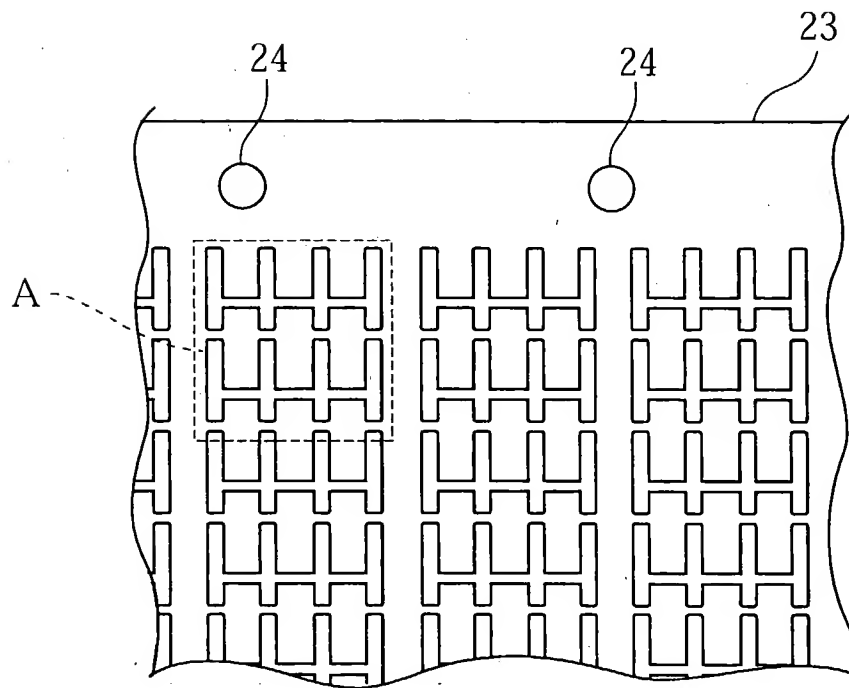


FIG.12

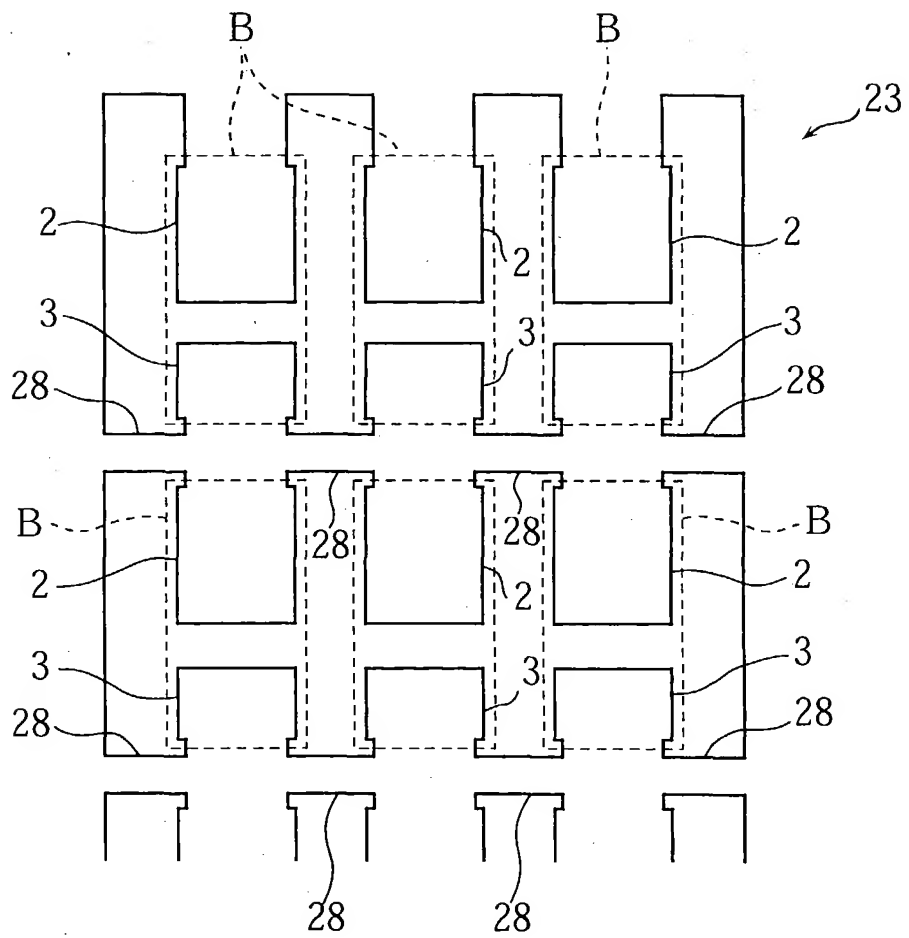


FIG.13

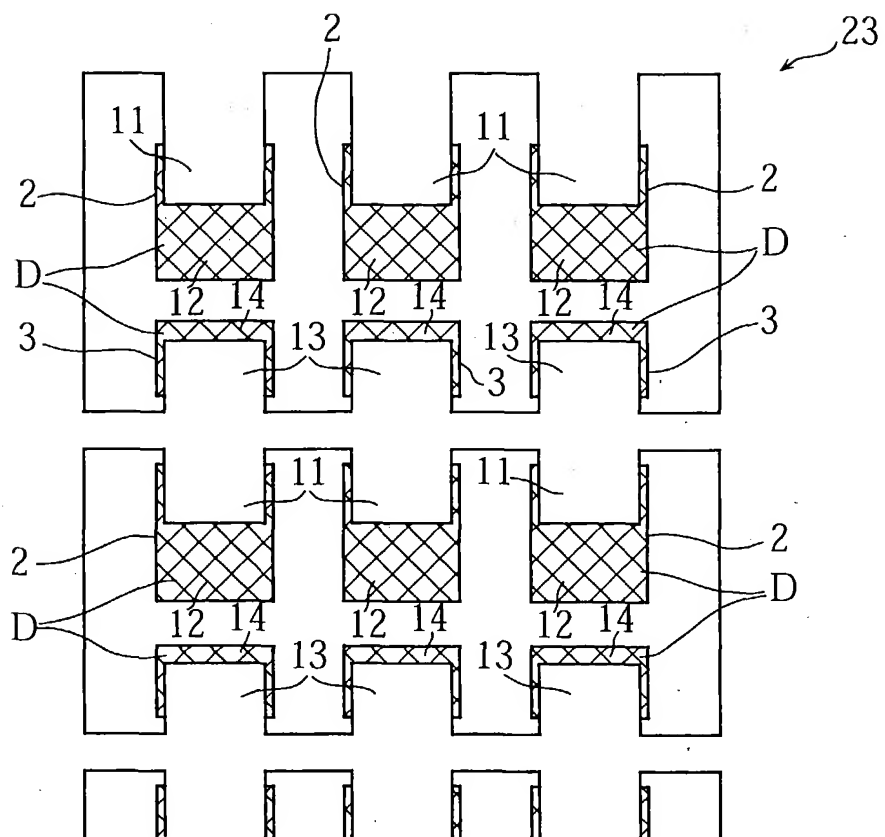


FIG.14

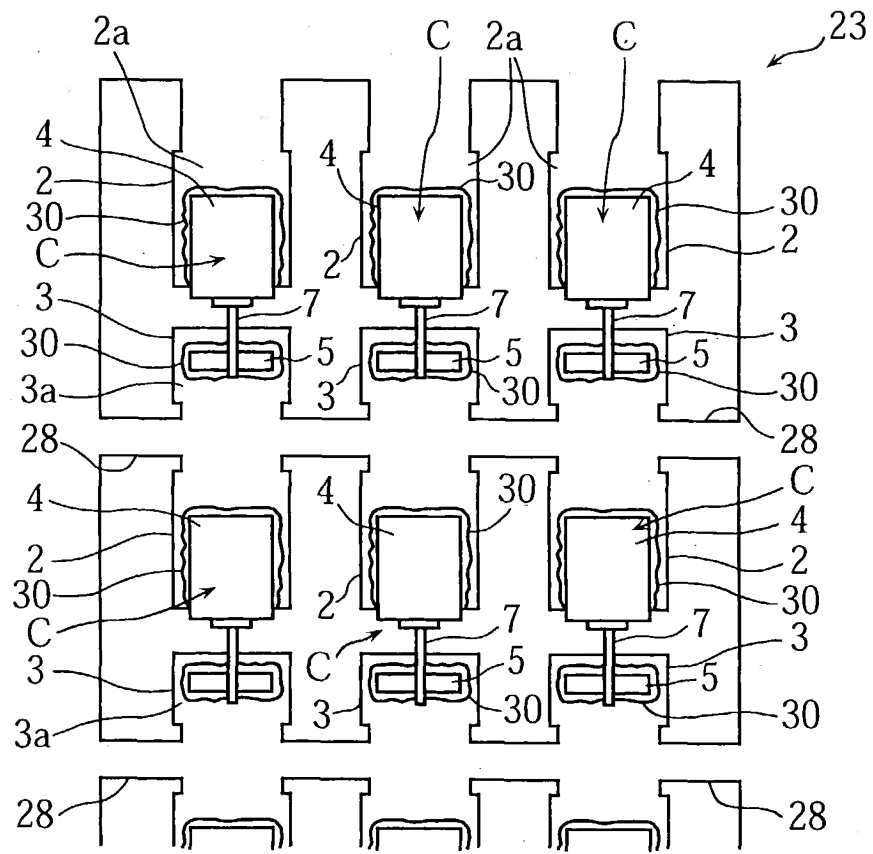


FIG.15

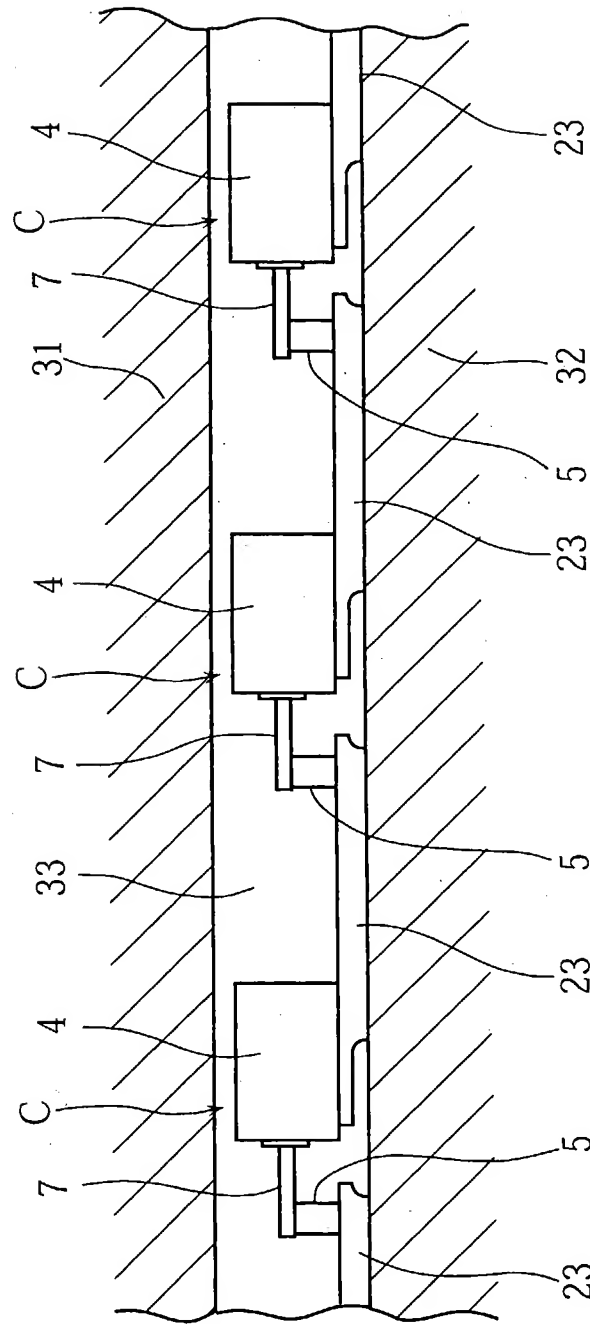


FIG.16

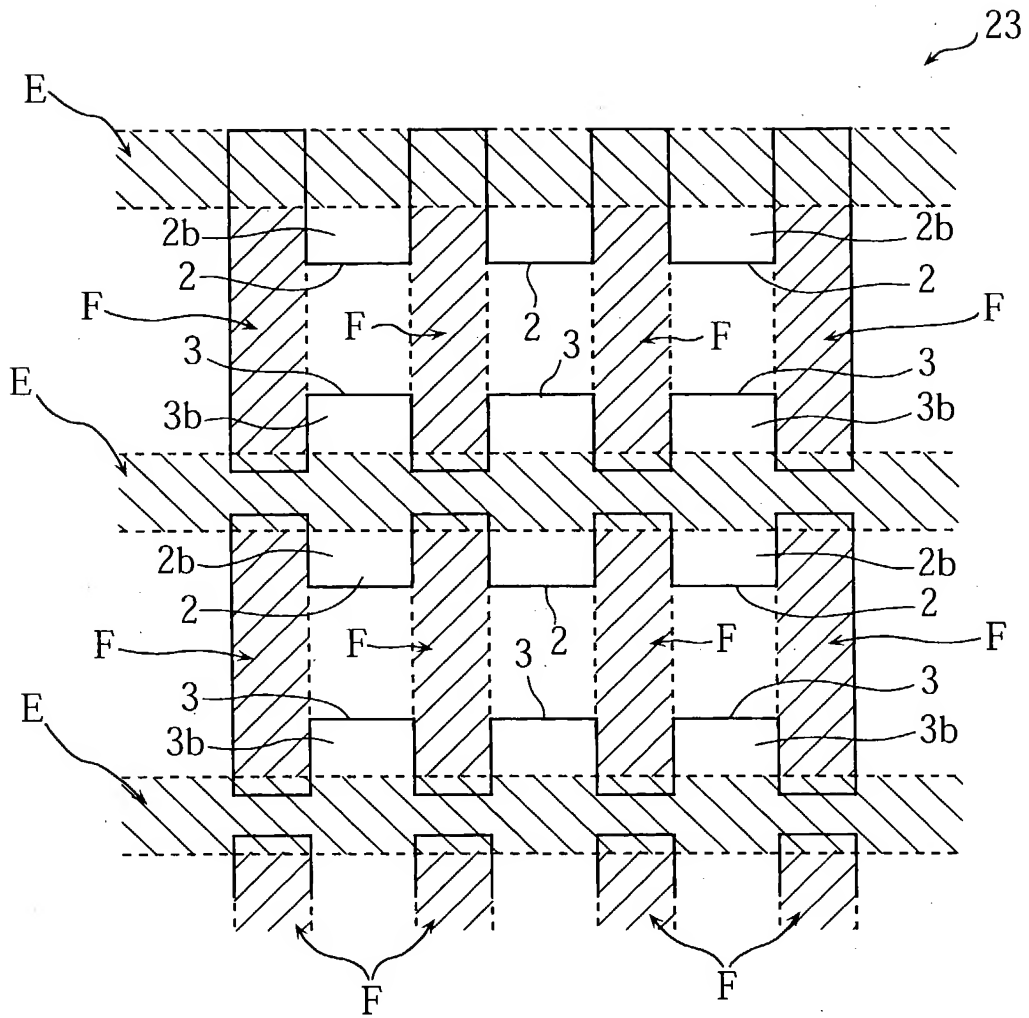


FIG.17

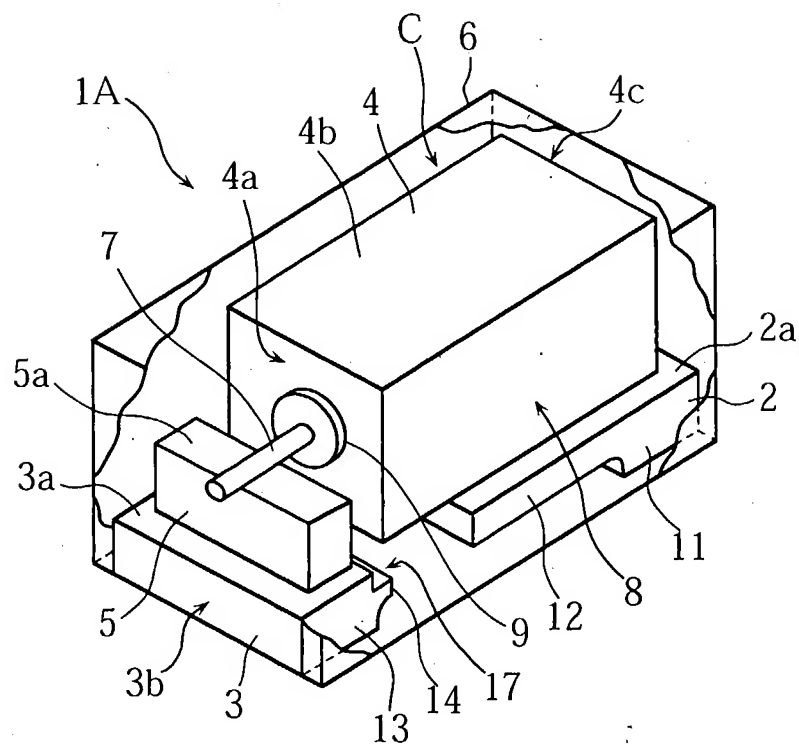


FIG.18

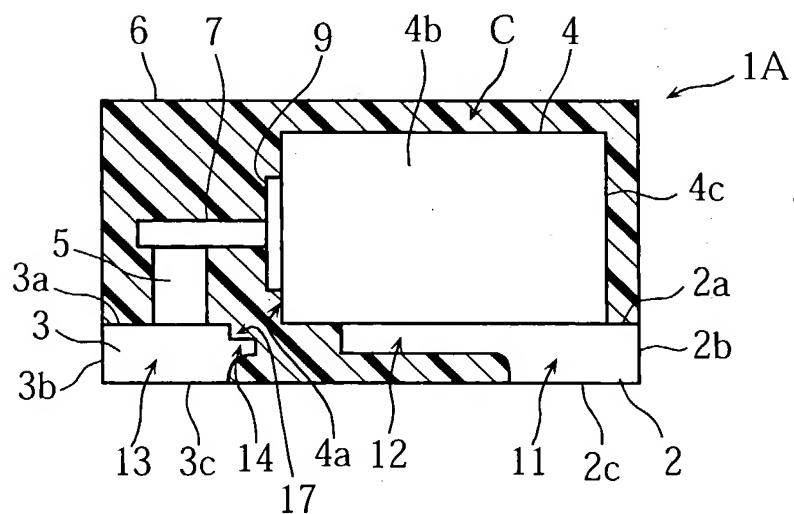


FIG.19

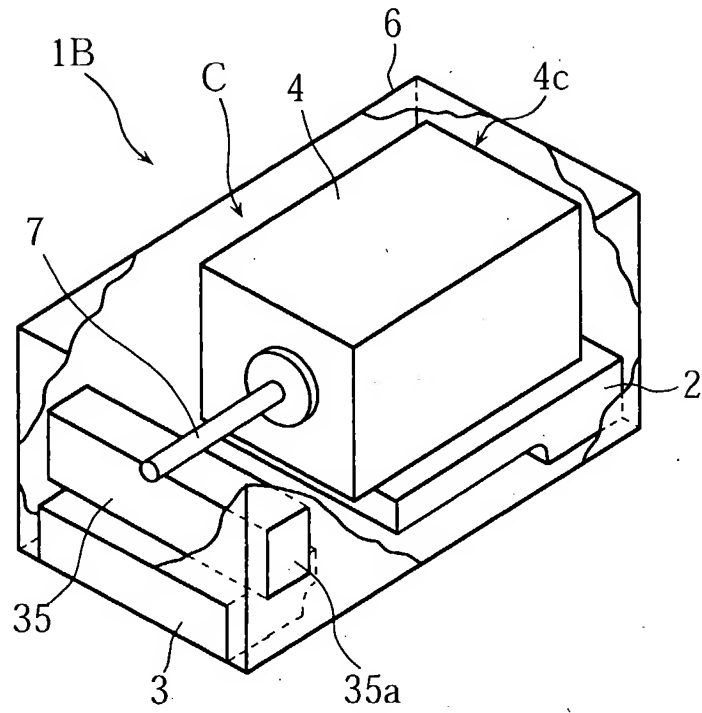


FIG.20

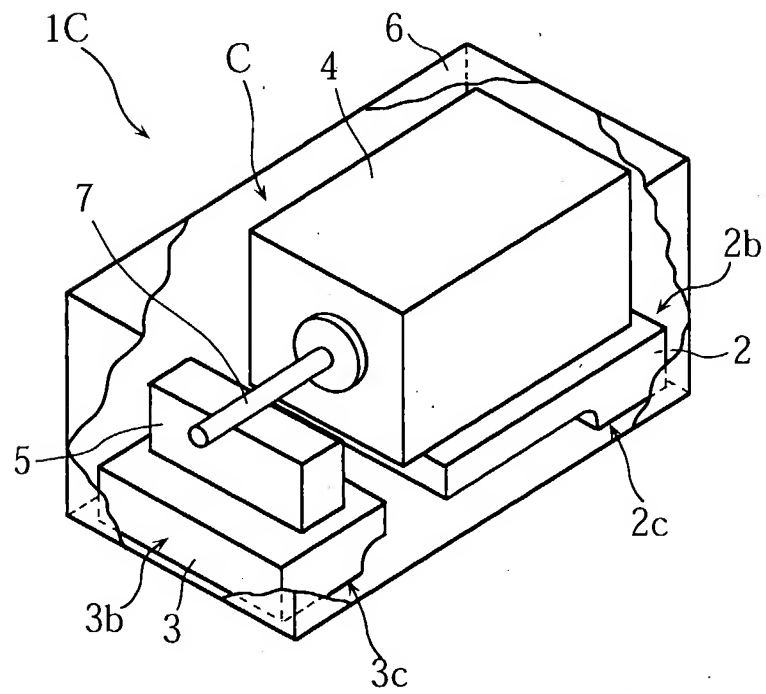


FIG.21

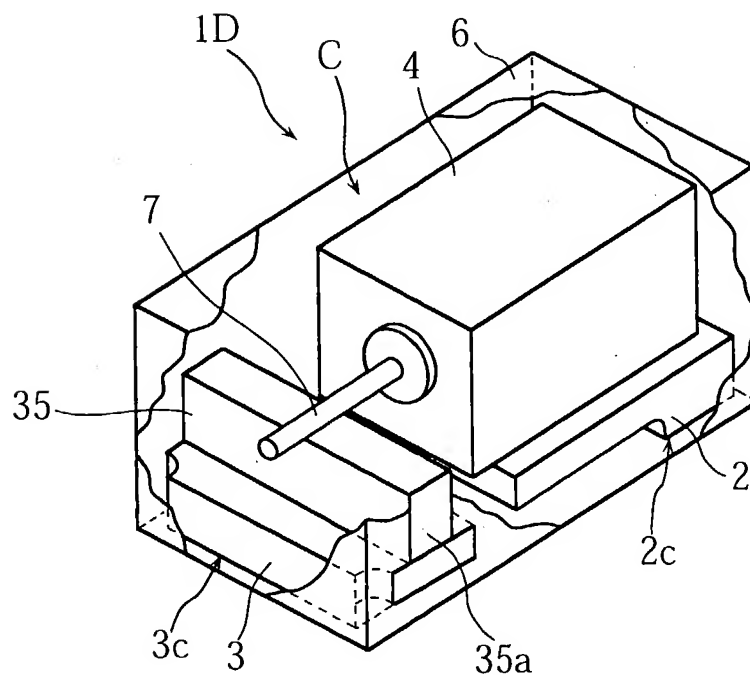


FIG.22

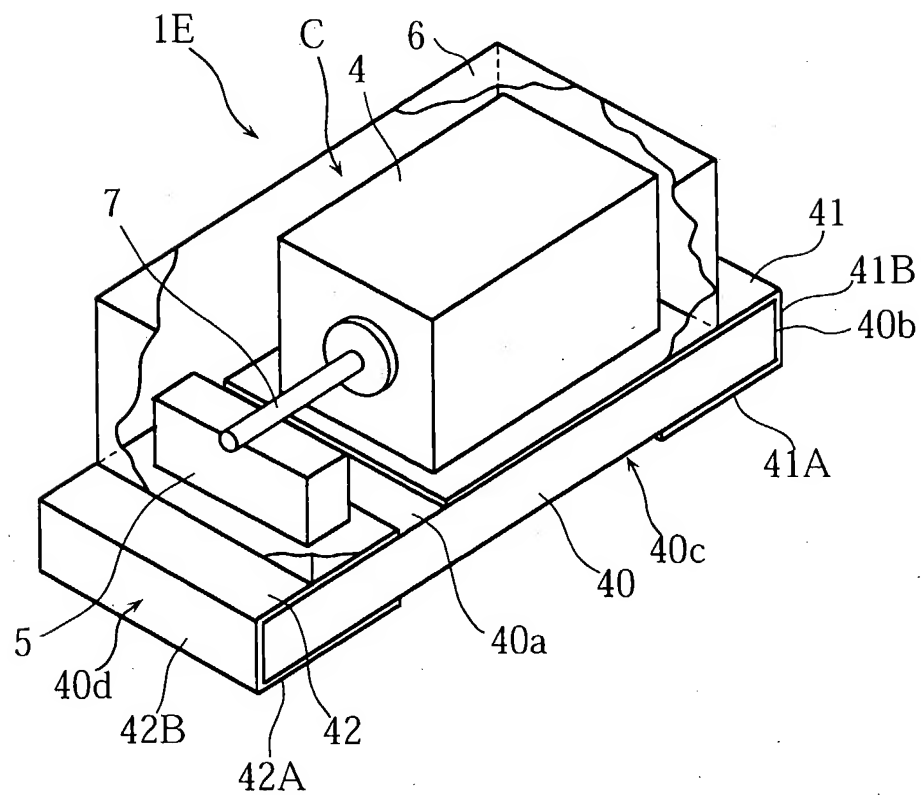


FIG.23

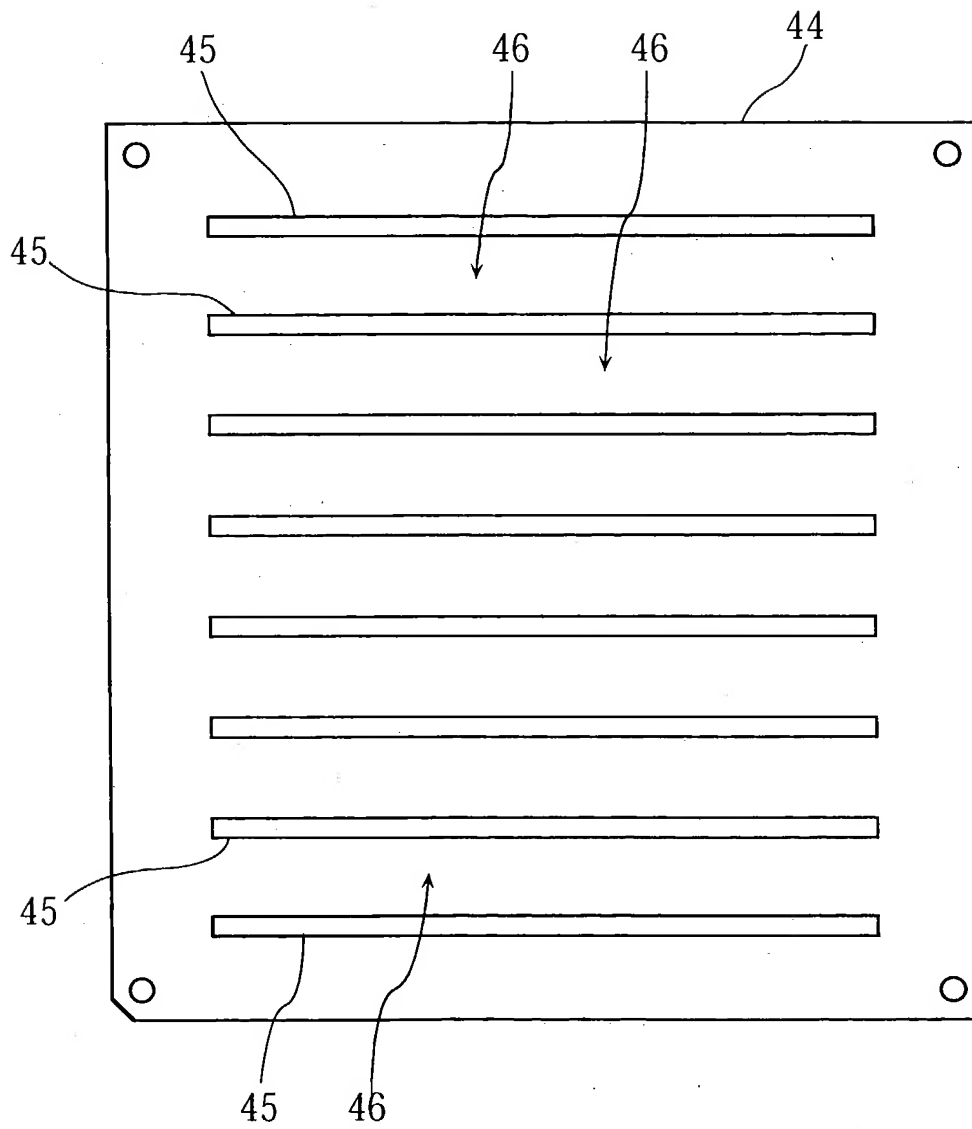


FIG.24

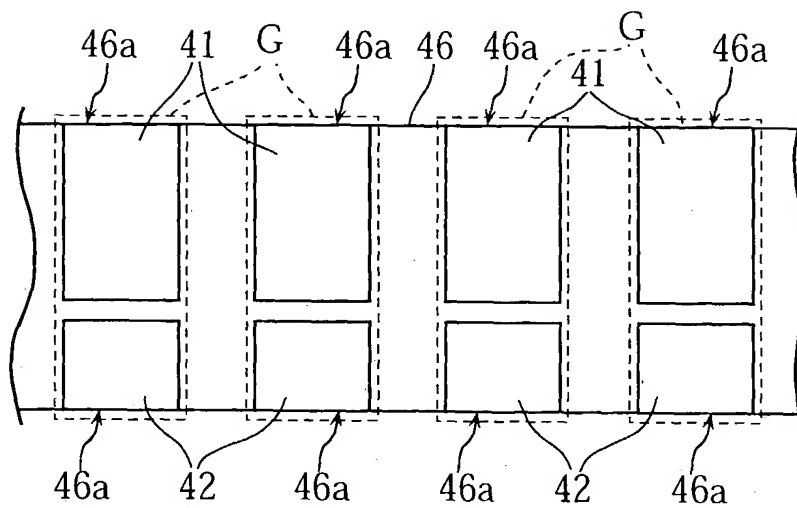


FIG.25

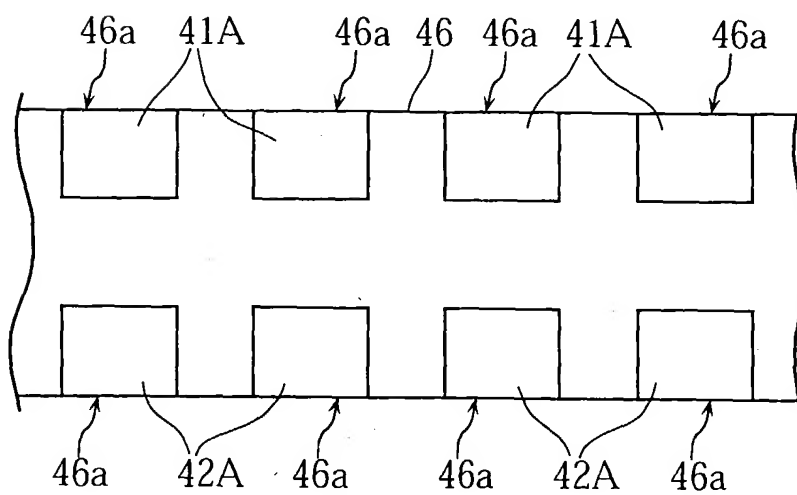


FIG.26

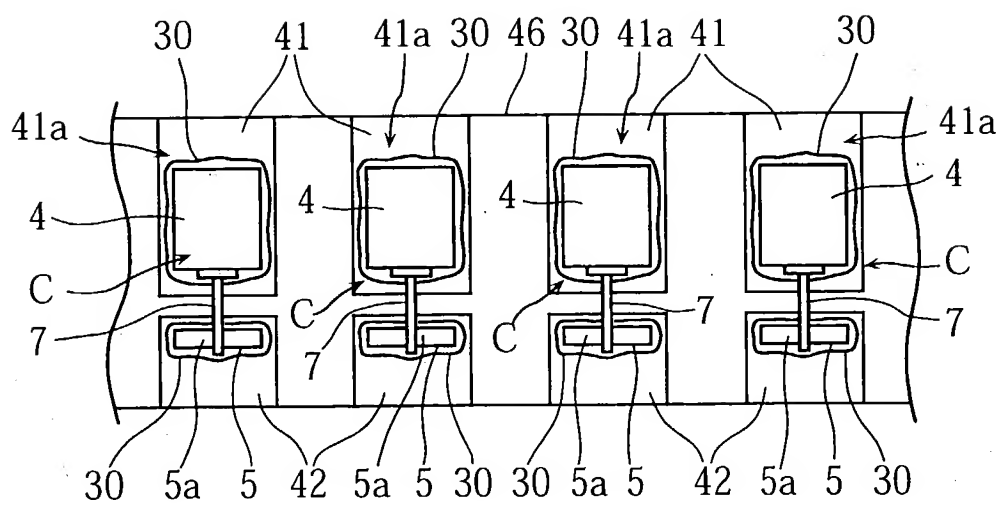


FIG. 27

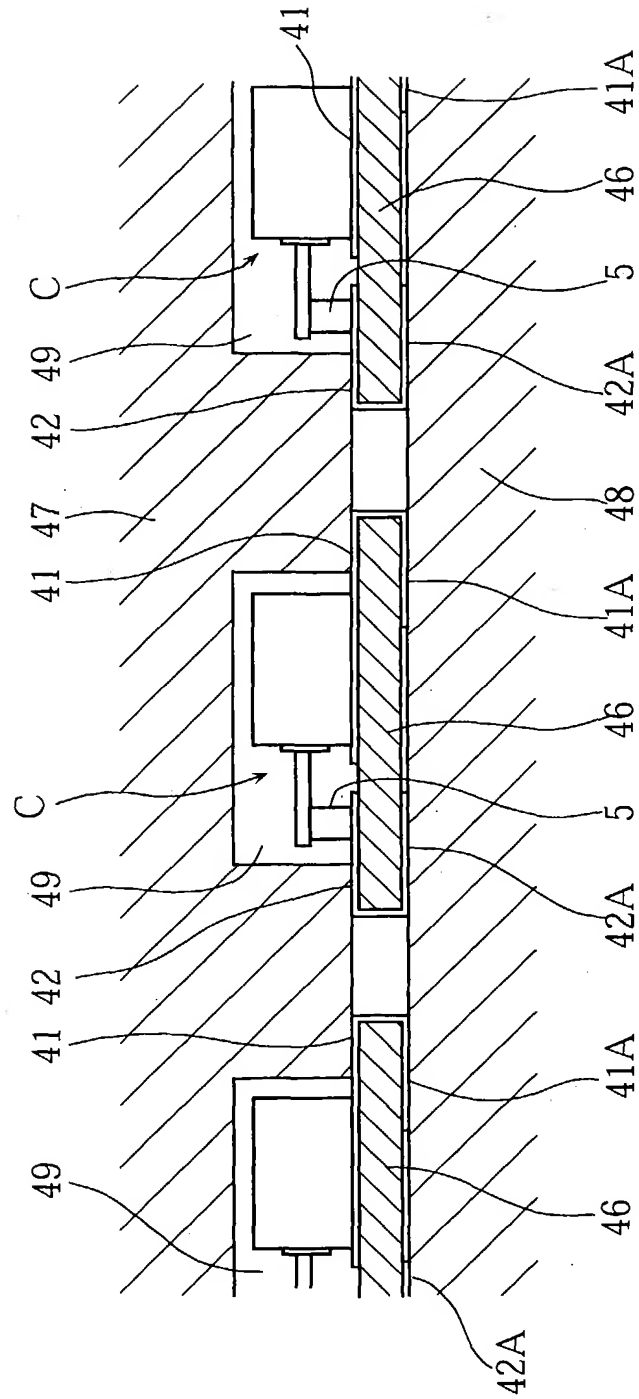


FIG.28

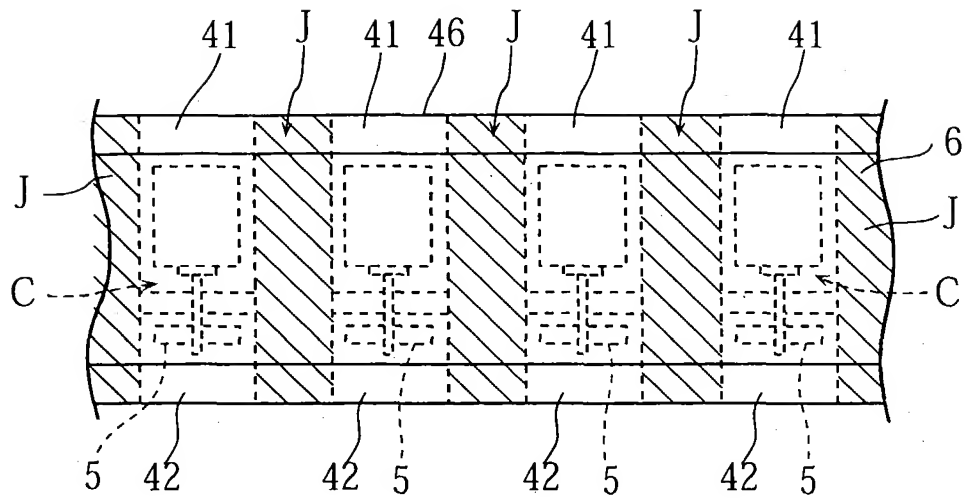


FIG.29

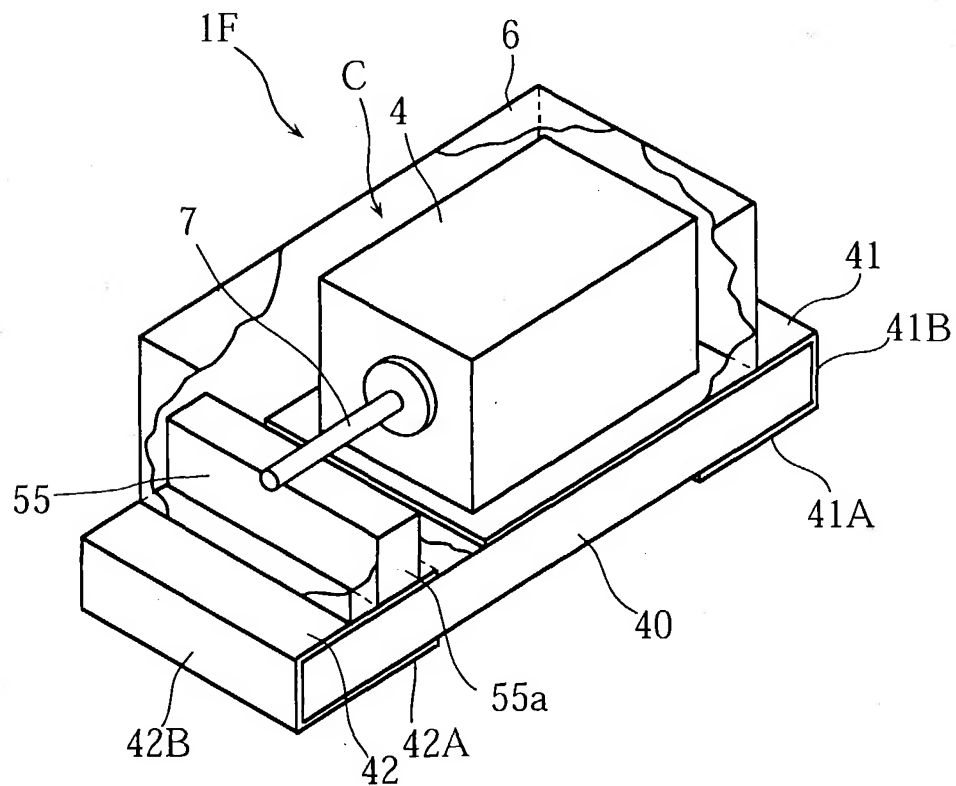


FIG.30

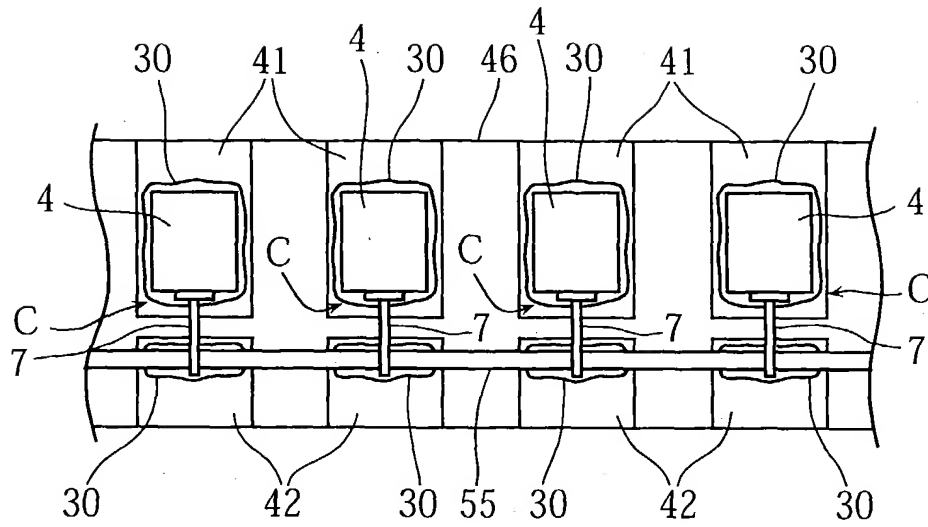


FIG.31

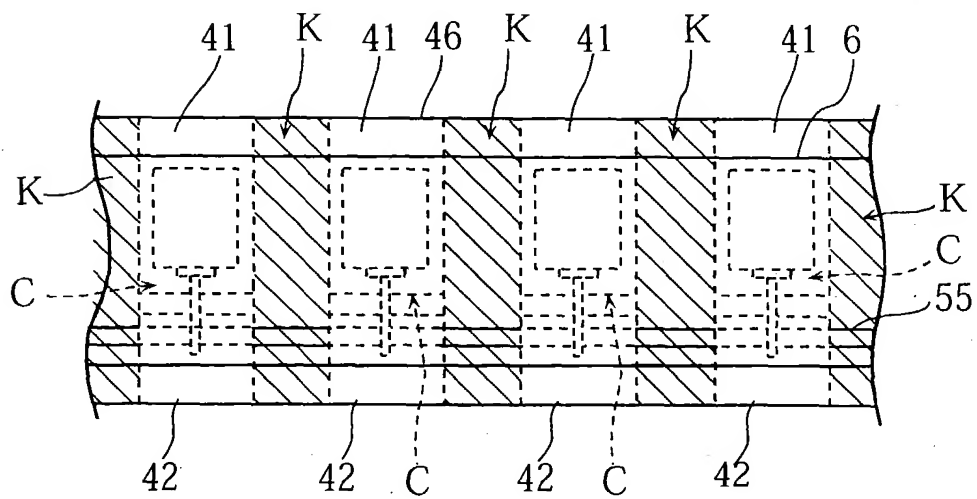


FIG.32

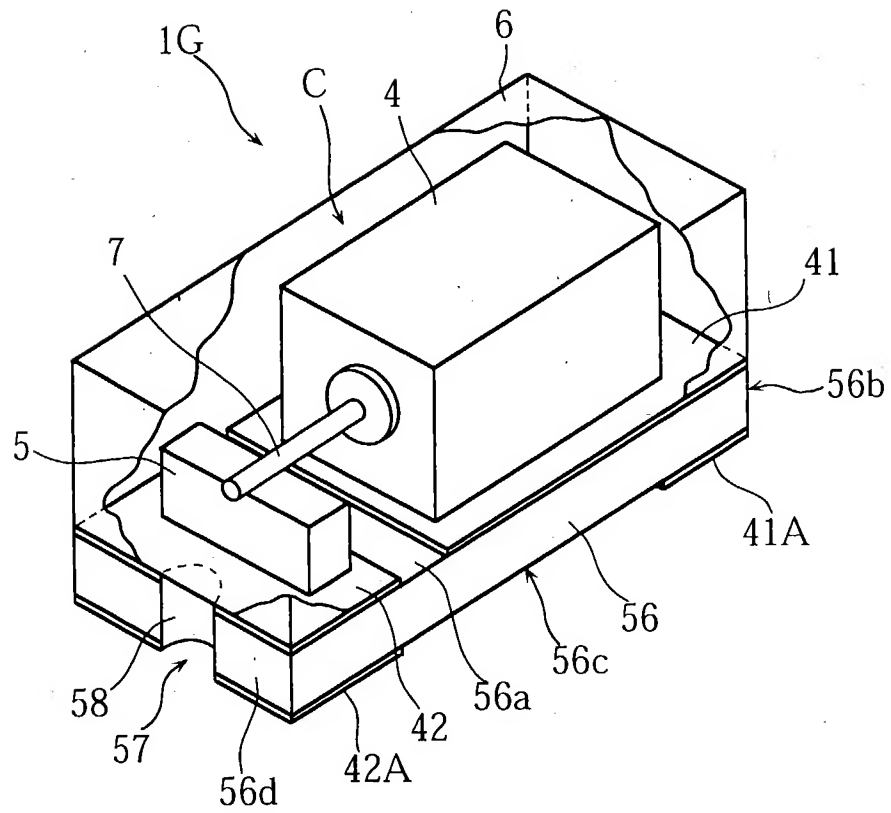


FIG.33

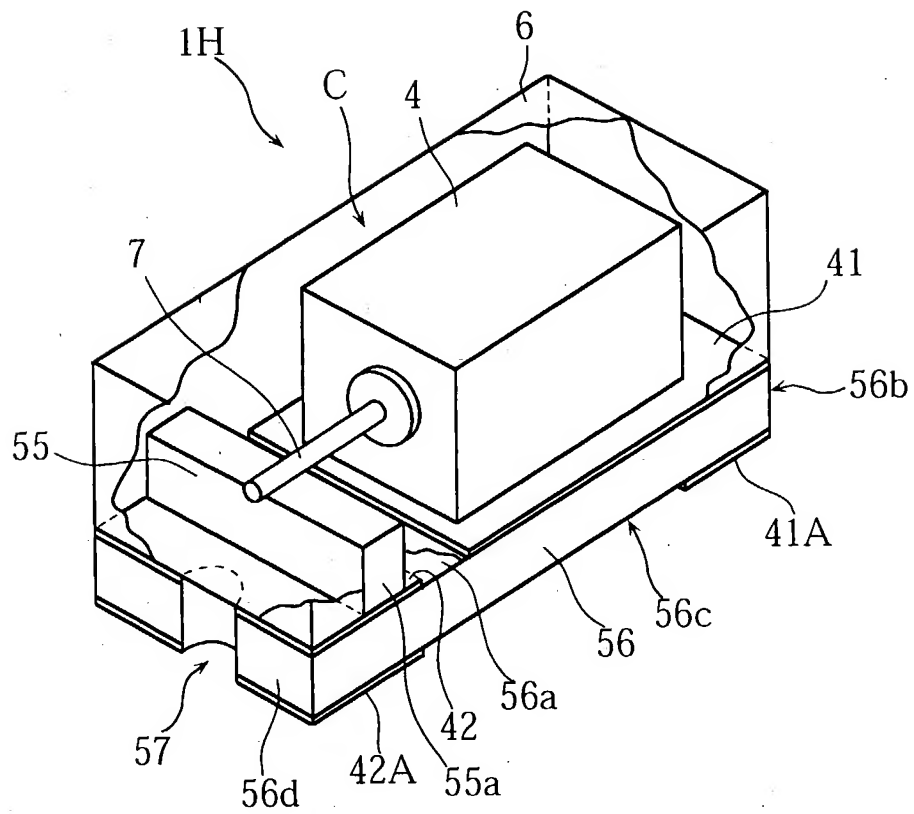


FIG.34
PRIOR ART

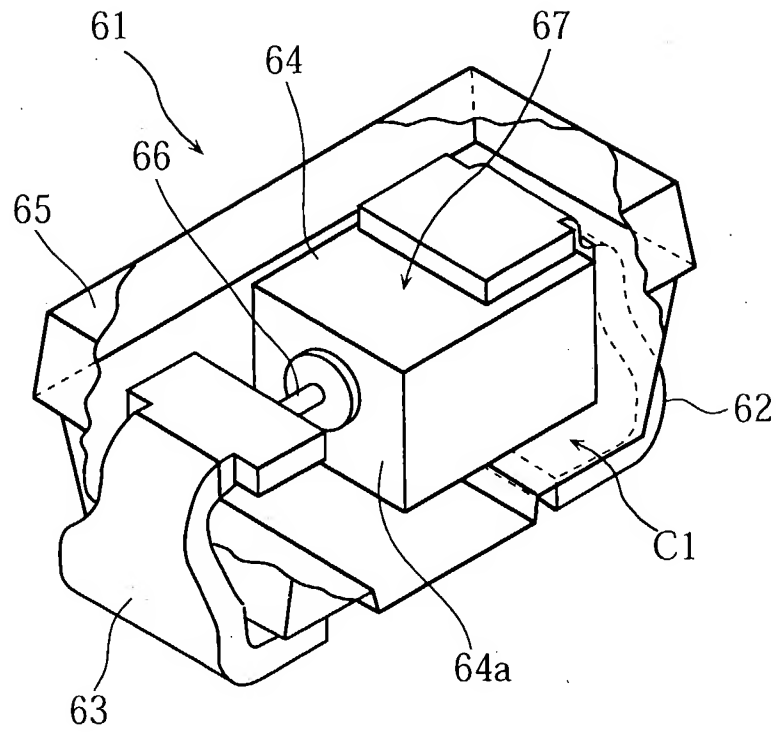


FIG.35
PRIOR ART

